IN THE CLAIMS

Please amend the claims to the following.

1 1. (Currently Amended) A system for maintaining cache coherency in a CMP

2   comprising:

3   an integrated circuit including

4   a plurality of processor cores, wherein the plurality of processor cores

5   each include a private cache;

6   a shared cache to be shared by the plurality of processor cores, wherein

7   the shared cache includes logic, in response to receiving a write

8   request referencing a block from a requesting processor core of the

9   plurality of processor cores and the block not being owned, ~~is~~ to

10   generate a first message, and wherein the first message when

11   received by a second processor core of the plurality of processor

12   cores is to invalidate the block in the ~~a~~ second processor core ~~of~~

13   ~~the plurality of processor cores~~ and the first message, when

14   received by the requesting processor core, is also to act as ~~provide~~

15   a write acknowledgement to the ~~a~~ requesting processor core~~, in~~

16   ~~response to receiving a write request referencing a block from the~~

17   ~~requesting processor core and the block not being owned~~; and

18   a ring to connect the plurality of processor cores and the shared cache, the

19   ring to transmit the first message to the requesting processor core

20   and second processor core.

1 2. (Canceled)

1 3. (Previously Amended)   The system of claim 1 wherein the shared cache

2   includes one or more banks, wherein the one or more cache banks is responsible

3   for a subset of a physical address space of the system, and wherein the block is

4   associated with a physical address of the physical address space of the system.

1 4. (Previously Amended)   The system of claim 1 wherein the first message

2   includes an InvalidateAndAcknowledge message , and wherein the shared cache

3   is to generate the InvalidateAndAcknowledge message, further in response to the

4   block being present in the shared cache and the second processor core being a

5   custodian for the block.

1 5. (Currently Amended) The system of claim 1 wherein the first message includes

2   an InvalidateAllAndAcknowledge message, and wherein the shared cache, in

3   response to receiving the write request referencing the block from the requesting

4   processor core of the plurality of processor cores and the block not being owned,

5   is to generate the InvalidateAllAndAcknowledge message, further in response to

6   the block not being present in the shared cache and none of the plurality of

7   processor cores being a custodian for the block. the processor cores are write-

8   thru.

1 6. (Previously Amended)   The system of claim 1 wherein the plurality of

2   processor cores writes data through to the shared cache.

1 7. (Previously Amended)   The system of claim 1 wherein the plurality of

2   processor cores each include a merge buffer, and wherein each of the merge

3   buffers are to coalesce multiple stores to a same block.

1   8.   (Previously Amended)   The system of claim 1 wherein the shared cache is to

2   fetch a second block from a memory and generate a write acknowledge message

3   to provide a write acknowledgement to the requesting processor core in response

4   to receiving a second write request referencing the second block, the second block

5   not being present in the shared cache and not being owned by any of the plurality

6   of processor cores.

1   9.   (Previously Amended)   The system of claim 8 wherein the shared cache is to

2   generate an evict message to evict a third block from an owning processor core

3   and generate a second write acknowledge message to provide a second write

4   acknowledgment to the requesting processor core in response to receiving a third

5   write request referencing the third block, the third block being present in the

6   shared cache and the owning processor core of the plurality of cores owns the

7   third block.

1   10.   (Previously Amended)   The system of claim 1 wherein a bank of the shared

2   cache is to be a home location for a non-overlapping portion of a physical address

3   space associated with the block.

1   11.   (Previously Amended)   The system of claim 7 wherein each private cache of

2   the plurality of cores are not to hold dirty data, and wherein each of the merger

3   buffers are to hold the dirty data.

1   12.   (Original) The system of claim 1 wherein the ring is a synchronous, unbuffered

2   bidirectional ring interconnect.

1   13.   (Previously Amended)   The system of claim 12 wherein the first message has a

2   fixed deterministic latency around the ring interconnect.

1   14.   (Currently Amended) An apparatus comprising:

2   an integrated circuit including: a plurality of cores and a shared memory

3   connected in a ring, the shared memory to be accessible by each of the

4   plurality of cores, wherein each of the plurality of cores includes a private

5   memory and a merge buffer to purge data to the shared memory, and

6   wherein the shared memory includes logic is to generate an evict message

7   referencing an address associated with to an owning processor core of the

8   plurality of cores in response to receiving a read request referencing the

9   address from a requesting core of the plurality of cores and the owning

10   processor core owning a block associated with the address.

1   15.   (Previously Amended)   The apparatus of claim 14, wherein the ring includes a

2   synchronous unbuffered bi-directional ring interconnect.

1   16.   (Previously Added)   The apparatus of claim 14, wherein the shared memory is a

2   shared cache including a plurality of blocks, and wherein the shared cache is

3   capable of holding each of the plurality of blocks in a cache coherency state.

1   17.   (Previously Added)   The apparatus of claim 16, wherein the cache coherency

2   state for each of the plurality of blocks is selected from a group consisting of (1) a

3   not present state, (2) a present and owned by a core of the plurality of cores state,

4   (3) a present, not owned, and custodian is a core of the plurality of cores state,

5   and (4) a present, not owned, and no custodian state.

1   18.   (Currently Amended) A system comprising:

2   a processor including: a plurality of cores and a shared memory to be coupled

3   together with an unbuffered bi-directional ring interconnect, wherein each

4   of the plurality of cores is to be associated with a private cache memory,

5   the shared memory is to be accessible by each of the plurality of cores,

6   and the shared memory is to include a plurality of blocks, each of the

7   plurality of blocks capable of being held by logic in the shared memory in

8   a not present state, a present and owned by a core of the plurality of cores

9   state, a present, not owned, and a core of the plurality of cores is a

10   custodian state, and a present, not owned, and no core of the plurality of

11   cores is a custodian state; and

12   a system memory associated with the processor to hold elements to be stored by

13   the shared memory.

1   19.   (Previously Amended)   The system of claim 18, wherein each of the plurality of

2   blocks is a home location for a subset of a physical address space.

1   20.   (Previously Amended)   The system of claim 19, wherein the shared cache is to

2   generate a first message to invalidate a requested block in all cores of the plurality

3   of cores except for a requesting core of the plurality of cores, in response to

4   receiving a write request referencing the requested block from the requesting core

5   and requested block being held in the present, not owned, and no core of the

6   plurality of cores is a custodian state.